Topic area: **CMMSP**

Issues for Stark shift tuning of phosphorous doped silicon Qubits

N. Suwuntanasarn[1], W.D. Hutchison[1], R. Bramley[2], A.R. Hamilton[3], E. Gauja[3], R.G. Clark[3]

[1] *Centre for Quantum Computer Technology, School of PEMS, The University of New South Wales @ ADFA, Canberra ACT 2600*
[2] *Research School of Chemistry, The Australian National University, Canberra ACT 0200*
[3] *Centre for Quantum Computer Technology, School of Physics, The University of New South Wales, Sydney NSW 2052*

e-mail of corresponding author: w.hutchison@adfa.edu.au

Introduction

Quantum computation, when realised, will revolutionise information technology. A range of quantised physical systems have been suggested as the possible basis for a quantum computer. A number of these have already been demonstrated to work at least for a few quantum bits (qubits). The challenge is to scale such devices to a usefully large number of **identical** qubits and overcome the difficulties of stability and error correction. A solid state quantum computer based on silicon has potential in terms of scalability and compatibility with existing electronic fabrications. Qubits based on nuclear spins, at low temperature, promise long coherence times but present non-trivial issues in terms of read out.

The Kane [1] model for a silicon based quantum computer proposes that the nuclear spins of individual phosphorus dopant atoms be the qubits. An external voltage applied to so-called 'A gates' would be used to control the phosphorus hyperfine field and hence the nuclear magnetic resonance (NMR) frequency of the qubits. It is well known that the electron spin resonance (ESR) spectrum of ^{31}P in silicon at low temperature is a hyperfine split doublet [2]. Therefore ESR is a sensitive and convenient way to probe for changes in the phosphorus hyperfine field. However, initial ESR measurements on (bulk) P doped (natural) silicon as a function of externally applied DC voltage at 5 K, presented here, somewhat surprisingly show no Stark shift. Further DC current measurements at 4.2 K show that this observation is not a fundamental problem but the result of slow time scale charge migration in the 10^{17} cm^{-3} doped silicon. (The relatively high doping level of 10^{17} cm^{-3} was originally chosen to give an average donor separation of ~20 nm as specified for the Kane J coupling model.)

Stark Shift Estimates

In the Kane model [1] an electric field applied to the 'A gate' is used to reduce the hyperfine interaction and hence the resonant frequency of the P nucleus. This work aims to verify this proposal experimentally. Kane suggested that a linear tuning parameter of –30 MHz V^{-1} was appropriate to a device with P atoms situated 20 nm below an finite 'A' gate on an essentially infinite substrate. However an ESR experiment on bulk P doped Si requires reference to a different calculation. The spin Hamiltonian for a P donor has the form;

$$\mathbf{H} = g_e \mu_B B \mathbf{S} - g_N \mu_N B \mathbf{I} + A\mathbf{I.S}$$

where the hyperfine coupling constant is $A = \frac{4}{3}\pi\mu_0\mu_B g_N \mu_N |\psi(0)|^2$

For P:**Si**, A ≅ 7.79 x 10^{-26} J or 117.6 MHz and therefore $|\psi(0)|^2$ = 4.3 x 10^{29} m^{-3}. Effective

mass (hydrogen like) theory (Kohn [3]) reproduces this expectation value only if a correction is made such that $|\psi(0)|^2 \approx |\psi(r_s)|^2$.

Valiev and Kokin [4] use the Kohn theoretical approach exactly and proceed using perturbation theory to calculate the electric field dependence of A for a Kane computer-like scenario. In addition, they treat the case where the electric field in the vicinity of the P donor can be considered essentially uniform. This is the case for a bulk 'parallel plate capacitor type' measurement considered in this paper. The result obtained (in SI units) is:

$$\frac{\Delta A}{A} \approx -3.1 \text{ x } 10^{-16} E^2$$

Experimental Details

ESR was used in an attempt to observe experimentally a change in the hyperfine field of phosphorous doped into silicon, by an external voltage, as required for the Kane computer. For insulating P doped Si (~ 5 K and < ~3 x 10^{18} P/cm^3) the X-band ESR spectrum consists of just two lines hyperfine split by approximately A. Silicon wafers, 20 mm x 5 mm in area, ranging from 100 μm down to 60 μm thick (10^{17} P/cm^3) were prepared with ~500 nm of oxide followed by ~10 nm of Ti metal (covering the centre 19 mm x 4 mm) on the top and bottom surfaces. A 60 μm thick device was mounted in fixed frequency ESR spectrometer, using a specially designed KeL-F holder (no ESR signature) as shown in figure 1, and cooled to ~5 K with a helium flow cryostat. ESR was then recorded as a function of applied voltage. Based on the theoretical estimates, a ~0.1% change in hyperfine splitting would be expected for an applied voltage of 100 V in this configuration. Electrical measurements were made using a similar probe to cool ~100 μm thick wafers to 4.2 K in liquid helium bath.

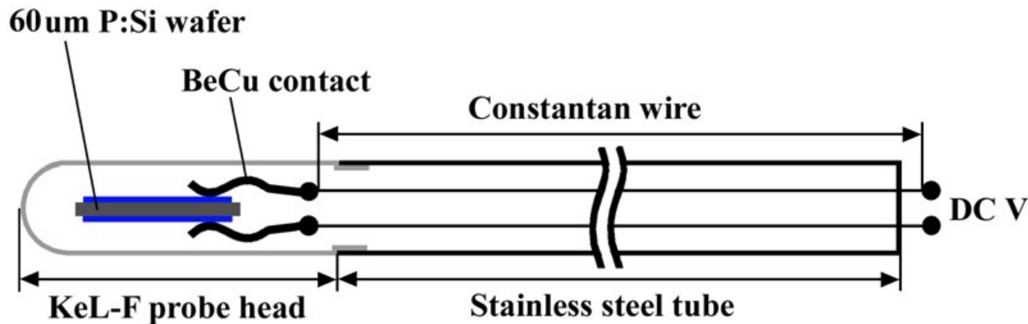

Figure 1. Mounting probe used for ESR and electrical measurements of thin wafers.

Results

Multiple ESR spectra were collected at ~5 K with voltages of 0, 50, 100, 150 and 175 V applied to a 60 μm wafer. Typical spectra (an applied voltage of 175 V compared with 0 V) are shown in figure 2. The average splitting at each voltage is compared with the theoretical relation in figure 3. Clearly no Stark shift is apparent experimentally.

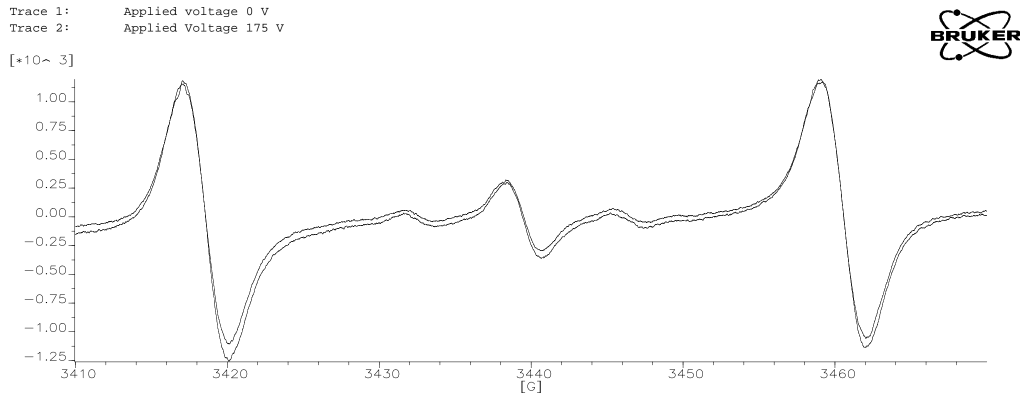

Figure 2. Typical ESR spectra at 5 K comparing results with 0 and 175 V DC applied.

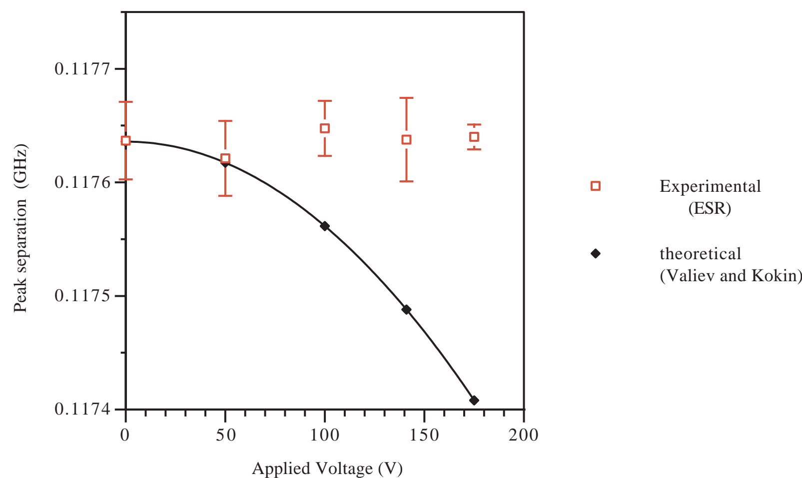

Figure 3. Experimental ESR hyperfine splitting for a 60 μm P doped Si wafer parallel plate capacitor at 5 K vs applied DC voltage is compared with the theoretical expectation.

At helium temperature the P donors are nominally localised, this is reflected in the observed hyperfine split ESR spectra. The entire device should behave as a single parallel plate capacitor with the silicon as the dielectric (k = 12). A simple calculation, ignoring the thinner oxide layers, for a 4 mm x 19 mm, 100 μm thick device gives a capacitance of about 80 pF. If however, charge is as mobile in the wafer, as it would be at room temperature, the device would be more like two series capacitors with thin silicon oxide dielectrics (k = 4) and a calculated capacitance of ~1.3 nF. Therefore, if the application of a large DC potential causes ionisation within the silicon, this should be reflected in a large change in the capacitance of the device. AC measurements of capacitance of a number of devices at 4.2 K over frequencies from 50 Hz to 10 kHz and in the presence of DC voltages up to 200 V gave steady values consistent with this calculated capacitance. However when the DC switching current at 4.2 K was recorded with a digital oscilloscope the situation is different. Typical data of such measurements are presented in figure 4 and show the charging current for the device, mounted to a probe through a series 1 MΩ resistor, is characterised by two time constants. Initially, the device charges with a time constant RC ≈ 0.15 ms (R = 1 MΩ, C = $C_{wafer} + C_{probe}$ = 150 pF) as might be expected from AC results. However finite current then

persists on a much longer time scale. This more slowly decaying component of the current which is thought to reflect charge movement within the silicon, appears earlier and is larger when the switching is at higher potential. Corresponding discharge curves are characterised by time constants appropriate to the room temperature (i.e. conducting silicon) capacitance.

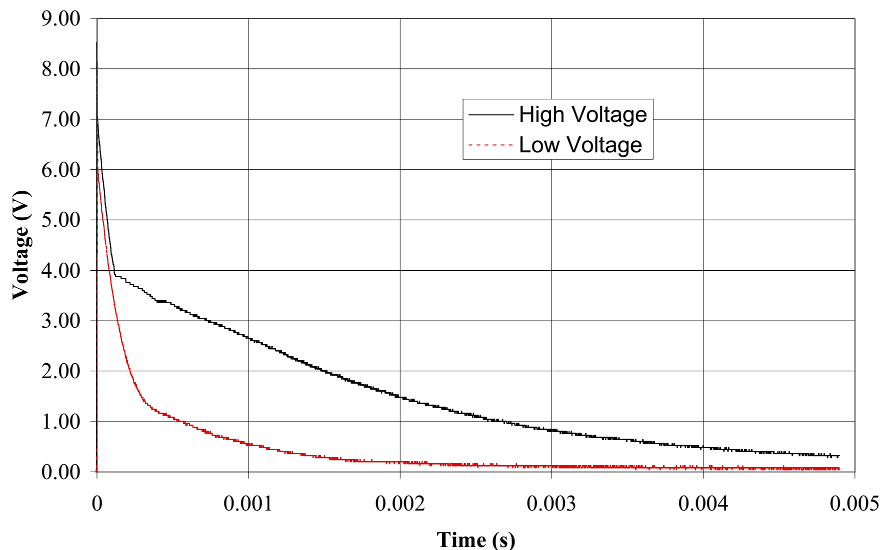

Figure 4. Charging current measured across a series 1 MΩ resistor for a probe mounted, 100 μm thick, oxidised and Ti coated wafer at 4.2 K. The low and high voltage curves are for switching from 0 to 9 V and 200 to 209 V respectively.

Discussion

ESR of the phosphorous donor in bulk silicon doped at a level of 10^{17} cm^{-3} as a function of DC electric field at low temperature does not reveal a Stark shift. The null result is, however not fundamental, but attributed to charge movement within the silicon, leading to shielding out of the applied electric field. This charge movement occurs on a relatively slow time scale and is evident for even quite modest E fields, as low as 9×10^4 V m^{-1}. The slow time scale suggests that it may be possible to observe the Stark shift in the present arrangement using an AC electric field at >10 kHz and such measurements are planned. Alternatively, use of silicon with a lower doping level would be likely to reduce the ionisation effects. Islands of donors in very close proximity are the probable source of electrons that cause further ionisation through impact.

Acknowledgements

This project is supported through the Centre for Quantum Computer Technology, an ARC Centre of Excellence. The following Centre staff are acknowledged for helpful discussions: A. Ferguson, D. McCamey, C. Wellard, L. Hollenberg and H. Goan.

[1] B. Kane, Nature **393**, 133 (1998).
[2] G. Feher, Physical Review **114**, 1219 (1959).
[3] W. Kohn, Solid State Phys. **5**, 258 (1957).
[4] K.A. Valiev and A.A. Kokin, quant-ph/9909008 \& Mikroelektronika **28**, 325 (1999).