Topic area: **CMMSP**

Practicality of Fault-Tolerant Quantum Computation

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Introduction

Recent analysis of Shor's algorithm [3, 4] has suggested that the practical implementation of large scale quantum algorithms will be heavily dependent on low effective error rates within any physical quantum computer. In particular the sensitivity of Shor's algorithm is such that any more than approximately 10-20 errors during the entire calculation for modest problem sizes leads to the algorithm failing to provide definitive output. For large factoring problems involving hundreds of physical qubits and millions of gate operations, this sensitivity to qubit errors is of great concern. Quantum error correction (QEC) and Fault-tolerant quantum computation (FTQC) provides a means to combat this problem. Many types of error correction codes have been developed, most notably the 9 qubit, 7 qubit and 5 qubit codes [2,5,6]. This paper examines the 7 qubit Steane code, since it is the most flexible when it comes to performing logical qubit operations directly on encoded data. Fault-tolerance is a specific method of working with these QEC codes in order to construct arbitrarily accurate circuits given the presence of either faulty components or environmentally induced errors. The threshold theorem for FTQC [1] is dependent on the unique nature of Fault-tolerant circuits, specifically, *a Fault-tolerant circuit is one such that a single error occurring at any location will at most cause a single error in the final output of the circuit.* This property of Fault-tolerance inevitably leads to complicated circuit structures in order to prepare logically encoded qubits, to perform correction and to implement specific single and multi-qubit gates. However, quantum error correction is able to be implemented non-Fault-tolerantly in a much simpler manner. Circuit structures for non-Fault-tolerant computation are generally much quicker, simpler and require less resources. The drawback is that threshold theorems for non-Fault-tolerant circuits are unavailable and hence error correction to arbitrary accuracy is not guaranteed. This paper examines the practicality of using Fault-tolerant circuits compared with their non Fault-tolerant versions. We will investigate the output fidelity of preparing a logical $|0\rangle$ state with the 7 qubit Steane code for a given error probability using a discrete error model. We will examine circuits appropriate for both a linear nearest neighbor (LNN) array of qubits and also an array that allows arbitrary coupling between qubits (non-LNN).

Circuits Needed for logical $|0\rangle$ encoding

The circuits required for both Fault-tolerant and non Fault-tolerant encoding are detailed in [1, 7]. Here we will present a few brief circuits used in this investigation. For both types of circuits

LNN and non-LNN, we assume that multiple pairs of qubits can be interacted simultaneously, provided that these pairs of qubits are isolated. For the following circuits we are also only considering the preparation of logical $|0\rangle$ states, since within general circuit design qubits do not undergo encoding while in superposition states. This also helps to simplify the circuits used for both Fault-tolerant and non-Fault-tolerant encoding. Figure (1) shows the basic circuits required for non-Fault-tolerant encoding of a logical $|0\rangle$ state for both the LNN and non-LNN arrays. Figure (2) details sections of the circuits required to encode Fault-tolerantly. The sections shown detail a single syndrome measurement. The entire Fault-tolerant circuit requires three of these syndrome measurements (performed on separate sets of four target qubits) which are run 2-3 times each depending on specific measurement results. More detail on these circuits can be found in [1]. It is clear that the Fault-tolerant versions of these circuits require a much larger number of qubits and gate operations. Table (1) summarises the resources required for each circuit.

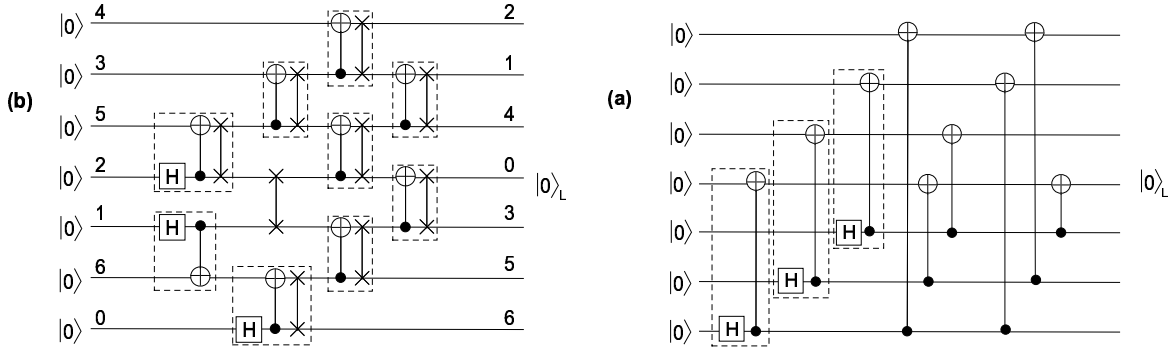

Figure 1: 7 qubit circuits for non-Fault-tolerant encoding. The figure (b) shows the circuit required for the LNN array while figure (a) details the circuit for a non-LNN qubit array. Dotted boxes represent compound gates that can be constructed via the canonical decomposition [8].

Circuit type	Number of Qubits	Depth	number of gate operations
LNN, non-FT	7	4	10
LNN, FT	12	96*	244*
non-LNN, non-FT	7	3	9
non-LNN, FT	12	60*	108*

Table 1: Resources required for various types of circuits to prepare a logical $|0\rangle$ state. * indicates the minimum possible depth and gate counts for Fault-tolerant circuits, since these circuits can change depending on specific measurement results obtained during the calculation.

The error model that was used in this investigation is the set of discrete errors, in which a single qubit $|\phi\rangle = \alpha|0\rangle + \beta|1\rangle$ can experience a bit flip $X|\phi\rangle$, a phase flip $Z|\phi\rangle$, or both at the same time $XZ|\phi\rangle$. Each of the three types of discrete error gates has an equal probability $p/3$ of occurring. For each circuit, p will be varied and output fidelity calculated. Output fidelity is defined as, $F = |\langle\phi|\phi'\rangle|^2$ where $|\phi'\rangle$ is the output wave-function from the circuit and $|\phi\rangle$ is the desired 7 qubit logical $|0\rangle$ state given by,

$$|\phi\rangle = |0\rangle_L = \frac{1}{\sqrt{8}}(|0000000\rangle + |1010101\rangle + |0110011\rangle + |1100110\rangle + |0001111\rangle + |1011010\rangle + |0111100\rangle + |1101001\rangle). \quad (1)$$

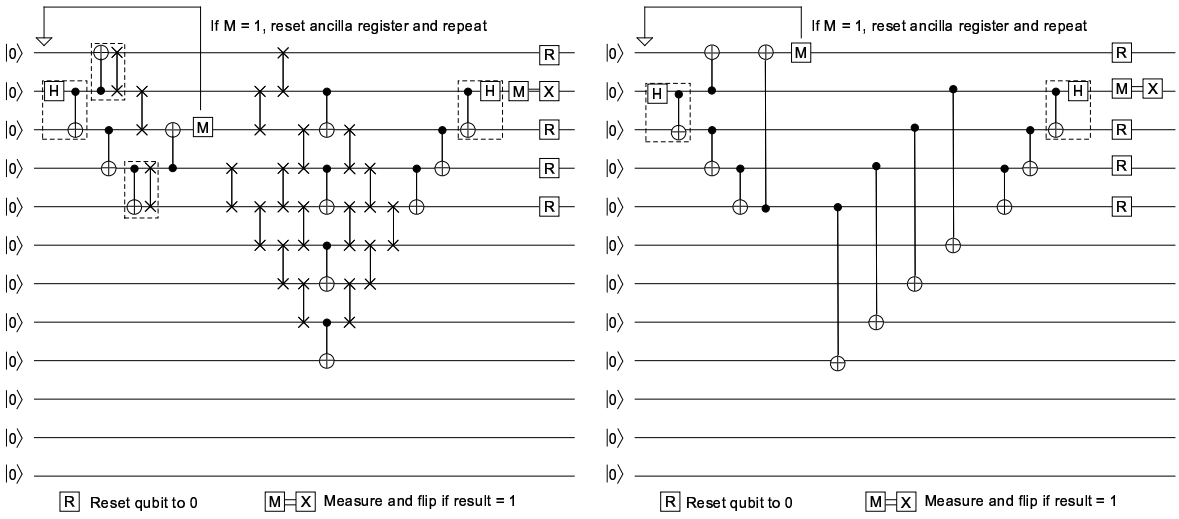

Figure 2: Section of the circuits required for Fault-tolerant encoding for LNN arrays (left figure) and non-LNN arrays (right figure). The section shown represents a single syndrome measurement. The entire circuit requires three such syndrome measurements that need to be performed 2-3 times depending on measurement results. Dotted boxes represent compound gates that can be constructed via the canonical decomposition [8].

Within Fault-tolerant circuits a single error anywhere within the circuit should only cause at most one error in the output which is then correctable. Hence, given a single error probability of p, a Fault-tolerant circuit should fail with probability p^2. This fact is clearly not true for the non-Fault-tolerant circuits. For example, any error proceeded by a CNOT operation will cause errors on both the target and control qubits. Hence simulations of the Fault-tolerant circuit consisted of a logical $|0\rangle$ preparation and a correction circuit. The correction circuit is essentially the same as the preparation circuit (again refer to [1] for more detail). We then compared the stability of this circuit with the non-Fault-tolerant preparation circuits shown in figure (1).

Results

The following figures show the results for both the LNN and non-LNN circuits. Figure (3) shows output fidelity vs probability of discrete error for the LNN circuits and non-LNN circuit respectively. The simulations were conducted in a stochastic manner with 10^6 statistical runs performed for each data point. Each plot shows a direct comparison between the Fault-tolerant and non-Fault-tolerant circuits.

From both plots it is clear that the non-Fault-tolerant circuit is generally more stable. At this stage the stochastic nature of these simulations don't allow for a detailed plot at extremely low error rates. A density matrix simulator is currently being finalised in order to find the crossover point where the Fault-tolerant circuits are more reliable than non fault-tolerant versions. However, we can still come to some reasonable conclusions as to the practicality of using Fault-tolerant computation for encoding. Currently accepted threshold rates for Fault-tolerant computation versus UN-encoded data lies in the region of $p = 10^{-5}$ to $p = 10^{-2}$. This is the error range in which experimentalists are currently aiming for in fabricated devices. This simulation data suggests that if we wish to use Fault-tolerant circuits for the encoding of qubits,

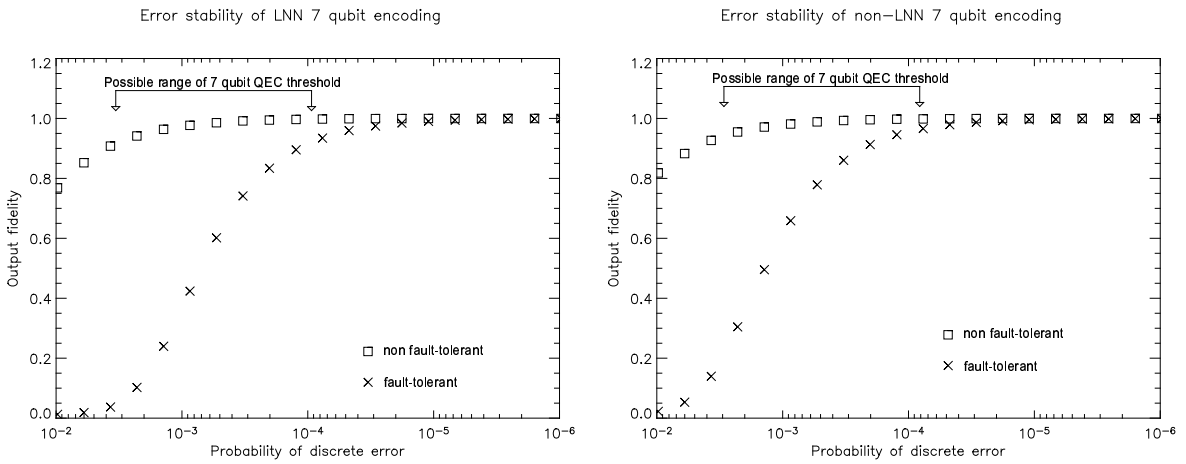

Figure 3: Stability of LNN (left plot) and non-LNN (right plot) 7 qubit encoding. Each curve shows output fidelity vs probability of discrete error for the Fault-tolerant encoding plus a correction stage, and the non fault-tolerant encoding. Non-Fault-tolerant encoding behaves better for all but extremely low error rates. Resolving these curves at low p is not possible due to long computational times.

that error rates of at least $p = 10^{-7}$ - 10^{-8} will be needed in order for Fault-tolerant circuits to be more reliable than their non fault-tolerant counterparts. Clearly the reason behind this major difference in stability between Fault-tolerant and non-Fault-tolerant circuits is caused by the massive increase in complexity required to encode qubits Fault-tolerantly. The total area of the circuits, given by $A = (\text{depth} \times \text{number of qubits})$ increases from just over 20 for the non-Fault-tolerant circuit to 300+ for the Fault-tolerant encoding and correction circuits. For a given probability of discrete error p, the larger area for the Fault-tolerant circuits increases the chance that multiple errors will occur compared to the very quick, non-Fault-tolerant encoding. It appears clear that for practical error rates, Fault-tolerant circuits to prepare logically encoded states are simply too complicated to be reliable. Either quicker and more efficient circuits or other QEC codes that can correct more than one error need to be developed or quantum circuits need to be designed using a combination of both Fault-tolerant and non-Fault-tolerant components such that maximum stability under errors is achieved.

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